## CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a substrate;

a plurality of metal layers, a first metal layer of said plurality of metal layers being

disposed on said substrate;

an inductor layer disposed within said plurality of metal layers; and

a circuitry for generating a negative capacitance, said circuitry

generating said negative capacitance of a value to compensate for a capacitance associated with metal layers adjacent to said inductor layer, said circuitry being coupled to said inductor layer.

2. The integrated circuit as claimed in claim 1, wherein a value of said negative capacitance is approximately equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer.

3. The integrated circuit as claimed claim 1, wherein said circuitry comprises:

at least two transistors;

at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors;

a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

4. The integrated circuit as claimed in claim 3, wherein said at least two transistors are at least one of bipolar transistors, MOSFETS, and gallium arsenide pseudomorphic high-electron mobility transistors.

5. The integrated circuit as claimed in claim 3, wherein said negative capacitance generated by said circuitry is dependent upon component values of said at least two resistors and said capacitor.

6. The integrated circuit as claimed in claim 1, wherein said circuitry is fabricated within the substrate.

7. An apparatus, comprising:

a housing;

a substrate disposed within said housing;

a plurality of metal layers, a first metal layer of said plurality of layers being disposed on said substrate;

an inductor layer disposed within said plurality of metal layers;

a circuitry for generating a negative capacitance, said circuitry generating said negative capacitance of a value to compensate for a capacitance associated with metal layers adjacent to said inductor layer, said circuitry being coupled to said inductor layer.

8. The apparatus as claimed in claim 7, wherein said value of said negative capacitance is approximately equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer.

9. The apparatus as claimed claim 7, wherein said circuitry comprises:

at least two transistors;

at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors;

a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

10. The apparatus as claimed in claim 9, wherein said at least two transistors are at least one of bipolar transistors, MOSFETS, and gallium arsenide pseudomorphic high-electron mobility transistors.

11. The apparatus as claimed in claim 9, wherein said negative capacitance generated by said circuitry is dependent upon a component values of said at least two resistors and said capacitor.

12. The apparatus as claimed in claim 11, wherein said negative capacitance generated by said circuitry is dependent upon a ratio of a first resistor to a second resistor multiplied by a value of said capacitor.

13. The apparatus as claimed in claim 7, wherein said circuitry is fabricated within the substrate.

14. An integrated circuit, comprising:

a substrate disposed within said housing;

a plurality of metal layers, a first metal layer of said plurality of metal layers being disposed on said substrate;

an inductor layer disposed within said plurality of metal layers;

a circuitry for generating a negative capacitance, said circuitry generating said negative capacitance of a value approximately equal in magnitude to a capacitance associated with metal layers adjacent to said inductor layer, said circuitry being fabricated within said substrate, said circuitry being coupled to said inductor layer.

15. The apparatus as claimed claim 14, wherein said circuitry comprises:

at least two transistors;

at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors;

a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

16. The apparatus as claimed in claim 15, wherein said at least two transistors are at least one of bipolar transistors, MOSFETS, and gallium arsenide pseudomorphic high-electron mobility transistors.

17. The apparatus as claimed in claim 15, wherein said negative capacitance generated by said circuitry is dependent upon component values of said at least two resistors and said capacitor.

18. The apparatus as claimed in claim 17, wherein said negative capacitance generated by said circuitry is dependent upon a ratio of a first resistor to a second resistor multiplied by a value of said capacitor.

19. An integrated circuit, comprising:

a substrate;

a plurality of metal layers, a first metal layer of said plurality of metal layers being disposed on said substrate;

an inductor layer disposed within said plurality of metal layers;

means for generating a negative capacitance, said generating means generating said negative capacitance of a value to compensate for a capacitance associated with metal layers adjacent to said inductor layer.

20. The integrated circuit as claimed in claim 19, wherein said value of said negative capacitance is approximately equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer.